PATENT CLAIMS

1. A flip-flop circuit arrangement, comprising

- a pair of input terminals (CP, CN), designed for supplying a differential clock signal,
- a pair of output terminals (QP, QN), designed for tapping a differential output signal,
- four differential amplifiers (1, 2, 3, 4), each having two transistors (5, 6; 7, 8; 9, 10; 11, 12), whose controlled sections are each positioned in a series circuit with a resistor (R1, R2, R3, R4), the series circuits being positioned between a first supply potential terminal (VCC) and a first and/or second shared emitter node (E1, E2), whose control terminals are coupled to one another to form a D flip-flop structure and in which the pair of output terminals (QP, QN) is formed at the output of at least one differential amplifier (3),
- a first current source (Q1), which connects the first shared emitter node (E1) to a reference potential terminal (VEE),
- a second current source (Q2), which connects the second shared emitter node (E2) to the reference potential terminal (VEE),
- a first switch (S1), whose controlled section is connected between the supply potential terminal (VCC) and the first emitter node (E1), and
- a second switch (S2), whose controlled section is connected between the supply potential terminal (VCC) and the second emitter node (E2),
- the first and the second switches (S1, S2) each having a control terminal which form the pair of input terminals (CP, CN).

2. The flip-flop circuit arrangement according to Claim 1,
characterized in that
- a first differential amplifier (1) is provided, comprising a first pair of emitter-coupled transistors (5, 6) in the first emitter node (E1), whose collector terminals form a first circuit node (ON1) and a second circuit node (OP1) and whose base terminals are cross connected to their collector terminals,
- a second differential amplifier (2) is provided, comprising a second pair of emitter-coupled transistors (7, 8) in the second emitter node (E2), whose collector terminals are connected to the first circuit node (ON1) and/or to the second circuit node (OP1) and whose base terminals form a third circuit node (ON2) and a fourth circuit node (OP2),
- a third differential amplifier (3) is provided, comprising a third pair of emitter-coupled transistors (9, 10) in the second emitter node (E2), whose collector terminals are connected to the third circuit node (ON2) and/or to the fourth circuit node (OP2) and whose base terminals are cross connected to their collector terminals, and
- a fourth differential amplifier (4) is provided, comprising a fourth pair of emitter-coupled transistors (11, 12) in the first emitter node (E1), whose collector terminals are connected to the third circuit node (ON2) and/or to the fourth circuit node (OP2) and whose base terminals are connected to the second circuit node (OP1) and/or to the first circuit node (ON1).

3. The flip-flop circuit arrangement according to Claim 2,

characterized in that the first, the second, the third, and the fourth circuit nodes (ON1, OP1, ON2, OP2) are each connected via a resistor (R1, R2, R3, R4) to the supply potential terminal (VCC).

4. The flip-flop circuit arrangement according to one of Claims 1 through 3,
characterized in that the first, the second, the third, and the fourth differential amplifiers (1, 2, 3, 4) and the first and the second switches (S1, S2) are implemented in bipolar circuit technology.

5. The flip-flop circuit arrangement according to one of Claims 1 through 4,
characterized in that the first current source and the second current source (Q1, Q2) each comprise a transistor in metal oxide semiconductor circuit technology.

6. The flip-flop circuit arrangement according to one of Claims 1 through 5,
characterized in that it is implemented in emitter coupled logic circuit technology.